Claims

[c1] 1. A method for fabricating a raised source/drain of a semiconductor device, comprising:
forming a gate structure on a substrate;
forming a source/drain with a shallow-junction in the substrate beside the gate structure;
forming a spacer on sidewalls of the gate structure; and
forming an elevated SiGe layer on the gate structure and the source/drain with a shallow junction, wherein the elevated layer formed on the source/drain serves as an elevated source/drain layer.

[c2] 2. The method of claim 1, wherein forming the elevated SiGe layer comprises performing rapid thermal chemical vapor deposition (RTCVD) to form the elevated SiGe layer.

[c3] 3. The method of claim 2, wherein the RTCVD uses a reaction gas comprising Si_2H_6/GeH_4 mixture gas or SiH_2Cl_2/GeH_4 mixture gas.

[c4] 4. The method of claim 2, wherein the RTCVD is conducted under 1~20 Torr and 500 ° C.

[c5] 5. The method of claim 1, wherein a thickness of the elevated SiGe layer is 200~500 Å .

[c6] 6. The method of claim 1, further comprising performing an implantation to dope the elevated SiGe layer.

[c7] 7. The method of claim 1, further comprising forming a metal silicide layer on the elevated SiGe layer.

[c8] 8. The method of claim 7, wherein the metal silicide layer comprises cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

[c9] 9. The method of claim 1, wherein an implanting energy for forming the source/drain with a shallow junction is 2~3 KeV.

[c10] 10. A method for fabricating a raised source/drain of a semiconductor device,

comprising:

forming a gate structure on a substrate, the gate structure having a capping layer thereon;

forming a source/drain with a shallow-junction in the substrate beside the gate structure;

forming a spacer on sidewalls of the gate structure; and

forming an elevated SiGe source/drain layer on the source/drain with a shallow junction.

[c11] 11. The method of claim 10, wherein forming the elevated SiGe source/drain layer comprises performing rapid thermal chemical vapor deposition (RTCVD) to form the elevated source/drain layer.

[c12] 12. The method of claim 11, wherein the RTCVD uses a reaction gas comprising Si_2H_6/GeH_4 mixture gas or SiH_2Cl_2/GeH_4 mixture gas.

[c13] 13. The method of claim 11, wherein the RTCVD is conducted under 1~20 Torr and 500 ° C.

[c14] 14. The method of claim 10, wherein a thickness of the elevated SiGe source/drain layer is 200~500 Å .

[c15] 15. The method of claim 10, further comprising performing an implantation to dope the elevated SiGe source/drain layer.

[c16] 16. The method of claim 10, further comprising forming a metal silicide layer on the elevated SiGe source/drain layer.

[c17] 17. The method of claim 16, wherein the metal silicide layer comprises cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

[c18] 18. The method of claim 10, wherein an implanting energy for forming the source/drain with a shallow junction is 2~3 KeV.

[c19] 19. The method of claim 10, wherein the capping layer and the spacer comprise the same material.

[c20] 20. The method of claim 19, wherein the capping layer and the spacer both

comprise silicon nitride.

[c21] 21. A method for fabricating a raised source/drain of a semiconductor device, comprising:
forming a gate structure on a substrate, the gate structure having a capping layer thereon;
forming a source/drain with a shallow-junction in the substrate beside the gate structure;
forming a spacer on sidewalls of the gate structure;
forming an elevated SiGe source/drain layer on the source/drain with a shallow junction;
removing the capping layer; and
forming a metal silicide layer on the gate structure and the elevated SiGe source/drain layer.

[c22] 22. The method of claim 21, wherein forming the elevated SiGe source/drain layer comprises performing rapid thermal chemical vapor deposition (RTCVD) to form the elevated source/drain layer.

[c23] 23. The method of claim 22, wherein the RTCVD uses a reaction gas comprising Si_2H_6/GeH_4 mixture gas or SiH_2Cl_2/GeH_4 mixture gas.

[c24] 24. The method of claim 22, wherein the RTCVD is conducted under 1~20 Torr and 500 ° C.

[c25] 25. The method of claim 21, wherein a thickness of the elevated SiGe source/drain layer is 200~500 Å .

[c26] 26. The method of claim 21, further comprising performing an implantation to dope the elevated SiGe source/drain layer.

[c27] 27. The method of claim 21, wherein the metal silicide layer comprises cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

[c28] 28. The method of claim 21, wherein an implanting energy for forming the source/drain with a shallow junction is 2~3 KeV.

[c29] 29. The method of claim 21, wherein the capping layer and the spacer comprise different materials.

[c30] 30. The method of claim 29, wherein the capping layer comprises silicon oxide and the spacer comprise silicon nitride.